UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/935,283	08/22/2001	Brenor L. Brophy	5298-06300	8806

35617 7590 05/06/2004

CONLEY ROSE, P.C.
P.O. BOX 684908
AUSTIN, TX 78768

EXAMINER	
GANDHI, DIPAKKUMAR B	
ART UNIT	**PAPER NUMBER**
2133	5

DATE MAILED: 05/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/935,283	BROPHY ET AL.	
	Examiner	Art Unit	
	Dipakkumar Gandhi	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-22 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-22 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 22 August 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 1/23/2002.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1-2, 9-14, 16-20 are rejected under 35 U.S.C. 102(a) as being anticipated by Schneider (US 6,201,829 B1).

Schneider anticipates claim 1.

Schneider teaches a system for testing an integrated circuit (col. 4, lines 48-51, Schneider), comprising:

A random bit generator adapted to produce a random pattern of bits, at least a portion of which are configured to be clocked in parallel onto n conductors at a first rate (figure 5, col. 8, lines 33-35, lines 40-41, lines 51-53, Schneider); and

Logic adapted to compare each of the random pattern of bits with each of the random pattern of bits after having been converted to a serial bit stream clocked at a second rate equal to n times the first rate (figure 5, col. 8, lines 51-67, Schneider).

- Schneider anticipates claim 2.

Schneider teaches the system wherein the generator produces a random pattern of m bits (figure 5, col. 8, lines 33-35, Schneider).

- Schneider anticipates claim 9.

Schneider teaches a serializer having an input and an output, wherein the input is couple to receive a random pattern of m bits clocked in parallel upon n conductors at a first rate, and wherein the output is coupled to produce a serial bit stream clocked at n times the first rate (figure 5, col. 8, lines 33-35, lines 40-41, lines 51-53, Schneider); and

A deserializer coupled to receive the serial bit stream via a loop back conductor selectably connected between the serializer and the deserializer (figure 5, col. 8, lines 53-55, Schneider); and

A comparator coupled to receive m bits from the deserializer and to compare each of the m bits from the deserializer to corresponding bits identical to the random pattern of m bits place on the input of the serializer for testing the serializer and the deserializer (col. 8, lines 21-29, lines 60-67, Schneider).

- Schneider anticipates claim 10.

Schneider teaches the self-test circuit further comprising:

A clock generator coupled to selectively forward a first clock transitioning at the first rate to the serializer for synchronously receiving the random pattern of m bits (col. 6, lines 55-65, Schneider); and

A first phase-locked loop coupled to receive the first clock and to multiply the first rate by n to form a second clock transitioning at a second rate for clocking the serial bit stream (figure 5, col. 6, lines 66-67, col. 7, lines 1-2, Schneider).

- Schneider anticipates claim 11.

Schneider teaches the self-test circuit further comprising at least one relay coupled to selectively connect the loop back conductor between the serializer and the deserializer (col. 7, lines 58-63, Schneider).

- Schneider anticipates claim 12.

Schneider teaches the self-test circuit wherein the serializer comprises a transmit circuit coupled to accept the random pattern of m bits and transmit the serial bit stream (figure 5, col. 8, lines 33-35, lines 40-41, lines 51-53, Schneider); and wherein the deserializer comprises a receive circuit coupled to receive the serial bit stream and produce a plurality of frames consisting of m bits (col. 8, lines 1-4, Schneider).

- Schneider anticipates claim 13.

Schneider teaches the self-test circuit wherein the transmit circuit includes a phase locked loop having a multiply by n counter within a feedback loop of the phase locked loop (figure 5, col. 6, lines 66-67, col. 7, lines 1-2, Schneider).

- Schneider anticipates claim 14.

Schneider teaches the self-test circuit wherein the receive circuit includes a phase locked loop having a divide-by n counter within a feedback loop of the phase locked loop (figure 5, col. 7, lines 9-15, Schneider).

- Schneider anticipates claim 16.

Schneider teaches the self-test circuit wherein the serializer, the deserializer, and the comparator are interconnected upon a single semiconductor substrate (col. 4, lines 49-52, Schneider).

- Schneider anticipates claim 17.

Schneider teaches the self-test circuit wherein at least a portion of the serializer, the deserializer and the comparator comprise a programmable logic device (col. 7, lines 27-36, Schneider).

- Schneider anticipates claim 18.

Schneider teaches the self-test circuit wherein the m bits from the deserializer are arranged in a sequence identical to the m bits clocked in parallel upon the n conductors of the serializer such that the comparator compares the first bit within the sequence from the deserializer with respective bits within the random pattern of m bits (col. 7, lines 58-67, col. 8, lines 1-4, Schneider).

- Schneider anticipates claim 19.

Claim 19 follows the same limitations as claim 9. See rejection to claim 9, above. Claim 19 is rejected under the same rational as to claim 9 rejected above.

- Schneider anticipates claim 20.

Claim 20 follows the same limitations as claim 10. See rejection to claim 10, above. Claim 20 is rejected under the same rational as to claim 10 rejected above.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 3-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider (US 6,201,829 B1) in view of Yoshida et al. (US 5,444,645).

As per claim 3, Schneider teaches the system wherein the logic further comprises:

A frame compile circuit for gathering frames of m bits from the serial bit stream (figure 5, col. 7, lines 58-67, col. 8, lines 1-4, Schneider);

A comparator coupled to the frame compile circuit and the second random bit generator to receive the frames of m bits and compare each bit within the frames of m bits to respective bits within the second random pattern of bits (figure 5, col. 8, lines 21-29, Schneider).

However Schneider does not explicitly teach the specific use of a second random bit generator adapted to produce a second random pattern of bits identical to the random pattern of bits.

Yoshida et al. in an analogous art teach that a pseudo random pattern is generated by a pseudo random pattern generator identical in construction with the pseudo random pattern generator of each channel (abstract, Yoshida et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Schneider's patent with the teachings of Yoshida et al. by including an additional step of using a second random bit generator adapted to produce a second random pattern of bits identical to the random pattern of bits.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using a second random bit generator adapted to produce a second random pattern of bits identical to the random pattern of bits would provide the opportunity to compare the random pattern of bits transmitted and received and analyze the quality of the transmit and receive circuits.

6. Claims 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider (US 6,201,829 B1) and Yoshida et al. (US 5,444,645) as applied to claim 3 above, and further in view of Pailthorp et al. (US 4,941,082).

As per claim 4, Schneider and Yoshida et al. substantially teach the claimed invention described in claim 3 (as rejected above).

Schneider also teaches a signal indicating failure of a serializer which converts the random pattern of bits to the serial bit stream if each bit of frames of m bits are not at the same logic level as respective m bits of the second random pattern of bits (col. 8, lines 60-67, col. 9, lines 1-6, Schneider).

However Schneider and Yoshida et al. do not explicitly teach the specific use of a latch coupled to an output of the comparator for storing a signal.

Pailthorp et al. in an analogous art teach that the computed results appearing on the "P" output of multiplier/accumulator 98 are delivered to the inputs of the respective Xc output latch 108 and Yc output latch 106, which store the Xc and Yc signals (figure 7, col. 12, lines 65-68, Pailthorp et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Schneider's patent with the teachings of Pailthorp et al. by including an additional step of using a latch coupled to an output of the comparator for storing a signal.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using a latch coupled to an output of the comparator for storing a signal would provide the opportunity to store the qualification signal that can be used by the tester.

- As per claim 5, Schneider and Yoshida et al. teach the additional limitations.

Schneider teaches a deserializer which converts the serial bit stream to at least one parallel-delivered set of n bits placed onto another set on n conductors at the second rate divided by n (figure 5, col. 8, lines 1-4, Schneider).

Schneider teaches a signal indicating failure of the deserializer if each bit of the frames of m bits, after having undergone deserialization, are not at the same logic level as respective m bits of the second random pattern bits (col. 8, lines 60-67, col. 9, lines 1-6, Schneider).

Pailthorp et al. teach a latch coupled to an output of the comparator for storing a signal (figure 7, col. 12, lines 65-68, Pailthorp et al.).

7. Claims 6-7, 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider (US 6,201,829 B1) as applied to claim 1 above, and further in view of National Semiconductor Corp., "SCAN921023 and SCAN921224 20-66 MHz 10 Bit Bus LVDS Serializer and Deserializer with IEEE 1149.1 (JTAG) and at-speed BIST", February 2001, pp 1-20.

As per claim 6, Schneider substantially teach the claimed invention described in claim 1 (as rejected above). Schneider teaches presenting the instruction to the generator for signaling production of the random pattern of bits (figure 5, col. 8, lines 33-35, lines 44-47, Schneider).

However Schneider does not explicitly teach the specific use of a test access port adapted to receive an instruction compliant with IEEE std. 1149.1.

National Semiconductor Corp. teaches IEEE 1149.1 Standard Test Access Port (block diagrams and 1st paragraph on page 1, National Semiconductor Corp.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Schneider's patent with the teachings of National Semiconductor Corp. by including an additional step of using a test access port adapted to receive an instruction compliant with IEEE std. 1149.1.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using a test access port adapted to receive an instruction compliant with IEEE std. 1149.1 would provide the opportunity to access the backplane or cable interconnects and provide the ability to verify differential signal integrity to enhance the system test strategy.

- As per claim 7, Schneider and National Semiconductor Corp. teach the additional limitations.

National Semiconductor Corp. teaches the system wherein the instruction is forwarded from a host computer operating from an application program compatible with IEEE std. 1149.1 (page 1, page 3, National Semiconductor Corp.).

- As per claim 21, Schneider and National Semiconductor Corp. teach the additional limitations.

Claim 21 follows the same limitations as claim 6. See rejection to claim 6, above. Claim 21 is rejected under the same rational as to claim 6 rejected above.

- As per claim 22, Schneider and National Semiconductor Corp. teach the additional limitations.

Schneider teaches the method wherein the comparing comprises forwarding a signal indicating functional failure status of the serializer and deserializer (col. 8, lines 60-67, col. 9, lines 1-6, Schneider).

National Semiconductor Corp. teaches an access port compatible with IEEE std. 1149.1 (page 1, National Semiconductor Corp.).

8. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider (US 6,201,829 B1) and National Semiconductor Corp., "SCAN921023 and SCAN921224 20-66 MHz 10 Bit Bus LVDS Serializer and Deserializer with IEEE 1149.1 (JTAG) and at-speed BIST", February 2001, pp 1-20 as applied to claim 7 above, and further in view of Greene et al. (US 2002/0147611 A1).

As per claim 8, Schneider and National Semiconductor Corp. substantially teach the claimed invention described in claim 7 (as rejected above).

However Schneider and National Semiconductor Corp. do not explicitly teach the specific use of the system wherein the application program comprises the JAM Standard Test and Programming Language (STAPL).

Greene et al. in an analogous art teach that the Java Virtual Machine (JAM) (a trademark of and available from Sun Microsystems, Inc.) is currently the most popular software that converts the Java intermediate language into machine language (page 12, paragraph 126, Greene et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Schneider's patent with the teachings of Greene et al. by including an additional step of using the system wherein the application program comprises the JAM Standard Test and Programming Language (STAPL).

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the system wherein the application program comprises the JAM Standard Test and Programming Language (STAPL) would

provide the opportunity to increase the processing speed of the application program, conduct the tests faster and reduce costs for testing devices.

9. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schneider (US 6,201,829 B1) as applied to claim 9 above, and further in view of Acton et al. (US 6,094,532).

As per claim 15, Schneider substantially teaches the claimed invention described in claim 9 (as rejected above).

However Schneider does not explicitly teach the specific use of the self-test circuit wherein the serializer, the deserializer, and the comparator are interconnected upon a single printed circuit board.

Acton et al. in an analogous art teach the printed circuit board having; a node ID, a memory moving device for reading data from the block sharable memory, a tagging device for tagging the block transfer with a destination node ID tag, a queuing device for queuing the tagged data, a serializer for serializing the queued data, a transmitter for transmitting the serialized data onto the serial bus to next successive processing node, a receiver for receiving serialized data from next preceding processing node, a deserializer for deserializing the received serialized data into parallel data, a sensor for sensing the destination tag within the parallel data, a comparator for comparing sensed destination tag with the node destination ID (col. 3, lines 24-35, Acton et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Schneider's patent with the teachings of Acton et al. by including an additional step of using the self-test circuit wherein the serializer, the deserializer, and the comparator are interconnected upon a single printed circuit board.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the self-test circuit wherein the serializer, the deserializer, and the comparator are interconnected upon a single printed circuit board would provide the opportunity to increase the data transmission speed and reduce the circuit costs.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 703-305-7853. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dipakkumar Gandhi
Patent Examiner

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100